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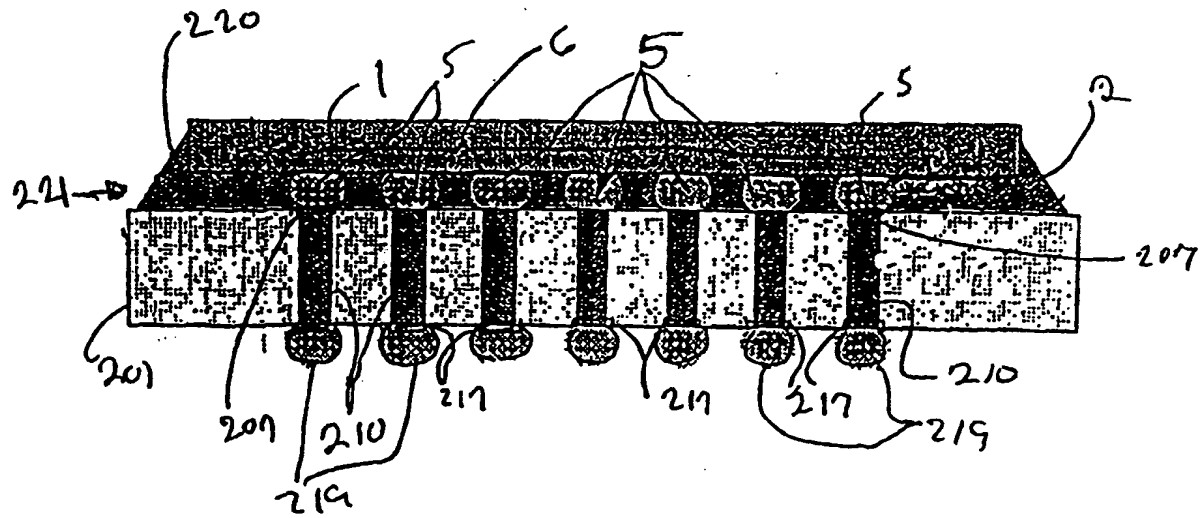

(57) Abstract

A chip scale package assembly (200) includes an integrated circuit die (1) having a number of input/output pads (3) formed about the periphery thereof. An array of contact pads (7) are disposed interior of the periphery of such die, each contact pad being coupled by conductive trace (8) to one of the input/output pads. A first set of conductive bumps (5) are formed upon the contact pads. A substrate (201) includes a plurality of conductive vias (210) extending therethrough and aligned with the first set of bumps. A first surface of the substrate lies adjacent the first set of bumps for allowing the conductive vias to be affixed thereto. A second set of conductive bumps (219) is formed on the opposing second surface of the substrate for attachment to a circuit. An underfill (220) may be applied to fill the gap (221) between the integrated circuit die and the substrate.

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FLIP CHIP AND CHIP SCALE PACKAGE

Technical Field

This invention pertains to integrated circuits, in general, and to flip chip integrated circuit devices and chip carriers therefor, in particular.

Background Art

Due to the numerous functions typically performed by the microcircuitry of integrated circuits, a relatively large number of input and output connections must be made to the microcircuitry. Most integrated circuit chips have bonding pads near their edges for the input/output connections. Locating the pads near the die edge is essential for wire and tape bonding.

A flip chip is, generally, a monolithic semiconductor integrated circuit device having bead-like terminals formed on the input/output pads. The terminals, also referred to as solder bumps, serve to both secure the chip to a circuit board and electrically interconnect the flip chip's integrated circuitry to a conductor pattern formed on the circuit board, which may be a ceramic substrate, printed wiring board, flexible circuit, or other substrate. Solder bumps are formed on the surface of the flip chip using methods such as electrodeposition or printing. The chip is then bonded to a conductor pattern on the circuit board by registering the bumps with their respective circuit board conductors and reheating or reflowing the solder so as to metallurgically bond the chip to the conductor pattern and thereby electrically interconnect each bump with its corresponding conductor.

Due to the manner in which the solder bumps are formed, the bumps are significantly wider than the corresponding pads. The size of a typical flip chip is generally on the order of a few millimeters per side. resulting in the solder bumps being crowded along the perimeter of the chip. Because of the narrow spacing required for the solder bumps and conductors, soldering a flip chip to its conductor pattern requires a significant degree of precision. The minimum spacing between bump is dictated by the required size of the bumps and the type of solder deposition process used. This spacing requirement imposes a minimum limit on the size of the flip chip die, regardless of the die area required for its circuitry. This spacing requirement can also preclude the conversion of existing die configured for fine pitch wire bonding to a solder bump flip chip.

One prior approach addressing the minimum spacing requirement of the bumps is described in U.S. Patent 5,547,740 in which an arrangement is described wherein solder bum are located a distance from the respective input/output pads. Electrically conductive runners extend from the input/output pads located adjacent the perimeter of the chip to bumps spaced apart from the perimeter. The solder bumps and runners can be formed after the device has completed all processing necessary to form either wirebond or flip chip integrated circuit. Th runners can be formed by including a photomask step to the processing that forms the solder contact without the requirement for an additional deposition and etching step.

One disadvantage of flip chip bonding is that a die change such as a change in size of tl die can force the designer to redesign the circuit layout. Another disadvantage relates to the differences in the thermal coefficients of expansion of silicon and to substrate materials such a the organic materials that are utilized in circuit boards. Repeated power cycling causes the solder bumps and ICs to fatigue and eventually fail. Such failures are less severe with face u mounted chips because the manufacturers can use permanently compliant material to fasten t chip to the substrate. Ceramic substrates improve flip chip reliability because they have therr coefficients of expansion which are closer to that of silicon and with silicon substrates the differences in the coefficients of expansion are negligible.

Although the integrated circuit chips may be directly bonded to circuit boards to elimir the use of a chip carrier, the integrated circuit chip is brittle and fragile and subject to stress a breakage if the circuit board has any flexing, or if the circuit board is vibrated or exposed to v variations in temperature. Chip scale packages (CSP) are integrated circuit chip carrier pack which are not significantly larger than the die itself, hence the term "chip scale".

A CSP device is less than 20% larger then the integrated circuit chip. CSP devices car be pre-tested and pre-speed sorted and do not require specialized testing or other processing common to bare die. Chip scale packaging offers the advantages of bare die design and assembly densities without the penalties common to bare die handling and assembly.

One problem with most CSP technologies is that the chip includes input/output pads disposed around and adjacent to the perimeter of the chip to permit wire bonding to the circu on a substrate. The bumps used for solder bumping to substrates are typically of a coarser or larger size than the input/output pads for wire bonding. The size is such that a significant risl adjacent bumps shorting out will occur if such bumps are used directly on the chip. One approach to solving this problem is to utilize a finer bump size on the chip and to affix the ch

to a substrate on which a redistribution of the input/output pads are repositioned to allow for appropriate spacing for the courser pitch for board assembly. The substrate is typically a laminate or ceramic material with subtractive and/or additive wiring. With peripheral pitches of less than 150Mm typical on integrated circuits today and with the attended routing requirements relatively expensive substrate technology must be used for this packaging approach.

It is desirable to provide a flip chip chip scale packaging arrangement in which redistribution of the chip input/output is achieved in such a manner as to permit the use of low cost substrates as the chip carrier.

Disclosure of the Invention

In accordance with the principles of the invention, a flip chip and chip scale package assembly is provided in which the chip may utilize closely spaced peripherally positioned input/output pads of the type and size that are utilized for wire bond connection and the input/output connections are redistributed.

In accordance with the principles of the invention, the input/output connections are redistributed on the chip by connecting each peripheral input/output pad to a corresponding one or a plurality of second pads arranged in a predetermined array. The connections are established by means of conductive paths which are disposed on the active surface side of the chip. The pads in the array are disposed so that the bumps placed on the pads may be of a coarser size needed to provide a bump connection to the conductors on the circuit board to which the chip is to be connected. A low cost substrate that has a corresponding array of through holes or "vias" is utilized. Each via is filled with conductive material. The vias are positioned on the substrate to be in registered alignment with the redistributed bumps on the flip chip. In accordance with the invention, the flip chip is bonded to the upper surface of the substrate by bonding the chip bumps to the vias on the substrate. The substrate includes an array of bumps disposed on the vias on the substrate lower surface. The bumps on the lower surface are or a coarse enough pitch to be directly mounted to circuit conductors.

Further in accordance with the principles of the invention an organic encapsulant may be utilized to fill the gaps between the flip chip and the chip scale substrate.

Brief Description of the Drawings

The invention will be better understood from a reading of the following detail description taken in conjunction with the drawing figures in which like designations are used to designate like elements, and in which:

Fig. 1 illustrates the active surface of a flip chip in accordance with the principles of the invention;

Fig. 2 illustrates a top view of a flip chip chip scale package in accordance with the invention;

Fig. 3 illustrates a bottom view of the flip chip chip scale package construction of Fig. 1;

Fig. 4 illustrates the flip chip chip scale package construction of Figs. 1, 2 and 3 taken in cross section along lines 4-4; and

Fig. 5 illustrates a typical solder bump utilized in the invention.

Best Mode for Carrying Out the Invention

A typical integrated circuit chip includes input/output pads disposed around the periphery of the chip. These input/output pads are provided to permit the wire bonding of the chip to terminal pins of an integrated circuit carrier package or in other instances to permit electrical connection to conductors in an electrical circuit by means of wire bonds. Fig. 1 illustrates the lower surface of a flip chip integrated circuit device 1 configured in accordance with the invention. The flip chip 1 is a silicon integrated circuit chip of conventional construction and includes an integrated circuit fabricated in one surface 2. The surface of the chip 1 upon which the integrated surface is formed is referred to as the active surface. As shc in Fig. 1, flip chip 1 includes a plurality of bond pads 3 disposed around the periphery of the c 1. As will be appreciated by those skilled in the art, the various Figures are provided for illustration purposes and are not drawn to scale. More specifically, each of the pads 3 is typically of such size and the pads 3 are disposed so close together such that it is difficult to provide solder bumps on the pads 3 of a coarse enough size so as to permit the bumps to effectively be used to connect to circuit conductors without risk of introducing electrical shor In accordance with the principles of the invention, an array 4 of bumps 5 are disposed in an interior area 6 of the chip. Each bump 5 is disposed on an electrical contact or pad 7, an illustrative one being shown in Fig. 5. Each of the interior pads 7 is connected to one of the corresponding input/output pads 3 by means of a conductive trace 8. As can be clearly seen i Fig. 1, the array 4 of bumps 5 is arranged such that the bumps formed thereon are spaced apa to eliminate any possibility of electrical shorts between adjacent bumps 5. As is also evident t those skilled in the art, the electronic circuitry which is formed on the chip 1 forms no part of present invention and may be any functional circuit.

Electrically conductive runners 8 serve to electrically interconnect the solder bumps 5 located apart from the perimeter of the device with their corresponding electrical contacts 3 located at the perimeter of the chip 1. The runners 8 are routed from the solder bumps 5 to the perimeter of the device 1, where the runners electrically connect pads 3 that are electrically interconnected with the integrated circuitry formed on the chip 1. Within the constraints of single level metal topography, a pad 3 at any location at the perimeter can be connected to a solder bump 5 at any location on the device.

Because adjacent input/output pads 3 are typically not required to be spaced sufficiently apart to accommodate solder bumps on each of their respective surfaces, the spacing between pads 3 along the perimeter of the device can be significantly reduced. Consequently, a greater number of solder bumps can be accommodated on a device having a given die size. Alternatively, a smaller die may be employed for a device requiring a given number of solder bumps.

The function and formation of the solder bumps 5 need not differ from that of the prior art. The solder bumps 5 can be formed by conventional techniques, then later reflowed to both bond the chip I to a substrate and provide the necessary electrical connections between the chip 1 and the substrate which functions as the chip scale package.

Fig. 5 illustrates the manner in which the redistribution may be accomplished on a conventional integrated circuit chip. The chip 1 includes an integrated circuit formed on surface 2 thereof.

A passivation layer 122 such as silicon dioxide, is formed on the surface of substrate 124. Prior to formation of the passivation layer 122, electrically conductive pads 3 are formed along the perimeter of the chip 1. A nitride layer 125 is formed after the conductive pads 3 are formed. Windows 126 are etched in the nitride layer 125 to permit access to the conductive pads 3. Typically, the conductive pads 3 may be aluminum or other suitable metal. To redistribute the electrical connections for the input/output access to the integrated circuit, runners 8 are formed such that their inward ends terminate where it is desired that a solder bump 5 be formed. To form the runners 8, a polymer layer 140 is deposited on top of the chip 1. The layer 140 is apertured in the areas of contacts 3 as well as in the areas of solderable contacts 7. A solderable contact 7 is then formed at the inward end of the runner 8 to electrically and physically interconnect each runner 8 to its corresponding solder bump 5. For this purpose, the solderable contact 7 is preferably composed of a copper layer 130 that will readily bond to the solder bump 5 and an intermediate nickel layer 131 and an aluminum layer 132. The nickel

layer 131 readily bonds to the aluminum layer and the copper layer, and also serves to preven the copper layer 130 from diffusing into the aluminum layer 132.

The solder bumps 5 can be screen printed or eclectrodeposited on the contacts 7. Suit solder alloys include, but are not limited to, tin-lead alloys containing about 60% tin, indium- alloys containing about 10 to 60% indium, and indium-lead-silver alloys containing about 10 60% indium and up to 5% silver.

Figures 2, 3 and 4 illustrate a flip chip chip scale package 200 assembled in accordance with the principles of the invention. In general, the construction shown includes the flip chip disposed on a chip scale package substrate 201. The substrate 201 may be of any conventior substrate material and, for example, may be a ceramic substrate, silicon substrate, or may be laminate, flex substrate or other material. The substrate 201 is sized such that its length and width are no greater than 120% of the corresponding length and width of the die 1. The thickness of the substrate 201 is a function of the type of substrate material used.

The substrate 201 has an array 204 of interconnection pads 207 that correspond to the array 4 of bumps 5 of the chip 1. The substrate material is typically a printed circuit board. Circuit boards are made from materials with low expansion coefficients are preferred (betwe about 6 and about 18 in/in/CX10^{-6}). One example of a useful material is Thermount E-215/C laminate from the DuPont Corporation of Wilmington, Delaware. This laminate is an epoxy resin reinforced with aramid fiber. Other types of organic resin such as polyesters, polyamid polyamides, and modifications or blends of these resins may also be employed in conjunction with aramid or other reinforcements. Other types of substrates such as alumina ceramic, beryllium oxide, or aluminum nitride may also be effectively employed.

The substrate 201 includes an array of conductive thru-holes or vias 210. The vias 21(are disposed to correspond both in number and position with the array 4 of bumps 5 carried the chip 1. Each via 210 is filled with a conductive material which may be a solder alloy, a m or a polymeric material. Metal pads 207 may be plated over the vias 210 utilizing conventior plating or deposition methods. The plating of pads 207 may be on both the upper and lower surfaces of the substrate. Pads 217 are provided at the bottom of each via 210. Bumps 219 applied to the pads 217 on the bottom surface of the substrate 201 utilizing the techniques described above or any other conventional method of applying bumps.

Although pads 207 are shown in its illustrative embodiment, other embodiments may deposit the bumps directly into the conductive vias 210.

In still a further embodiment, the vias 210 may comprise plated through holes rather than being filled with conductive material.

The flip chip 1 is bonded to the substrate 201 with the flip chip bumps 5 on the active 9 surface 2 being placed in registered alignment with the vias 210 on substrate 201. The bumps 5 are then bonded to the pads 207 utilizing any of the conventional bonding techniques known in the prior art including reflowing as shown in the aforementioned U. S. Patent 5,540,740. It should be noted that although the preferred embodiment of the invention utilizes solder reflow, a variety of other flip chip processes could be used to bond the chip 1 to the substrate 201 including isotropic or anisotropic conductive adhesive, thermocompression or compression bonds to attach the chip 1 to the substrate 201. In these alternate bonding techniques the bumps 5 may be made of conductive epoxy, conductive elastomer or other appropriate conductive material.

An organic fill or coupling agent 220 may be applied as an underfill in the gap 221 between the integrated circuit and the substrate 201. This may be, for example, a rigid adhesive such as an epoxy or a softer material such as an underfill silicone. An example of a suitable underfill is Hysol FP 4510, an epoxy from the Dexter Corporation of Industry, California. The underfill provides additional mechanical bonding between the device and the substrate, relieves stress and protects the active surface of the chip and the bump interconnections. The coupling agent may cover the entire gap between the device and the substrate or may only cover a portion of the active surface of the device. The integrated circuit chip 1 lies over the array of vias 210. Each via 210 connects to a solder pad 217 on the bottom side of the substrate 201. The underfill material 220 fills the gap between the chip 1 and the substrate 201. The input/output pads 3 of the chip 1 are electrically connected to the vias 210 of the substrate 201 by means of the array of bumps 5.

To summarize the formation of a flip chip chip scale package assembly in accordance with the invention is accomplished utilizing the following steps:

1. The input/output pattern of a flip chip 1 is redistributed from the periphery disposed pads 3 to an array 4 of pads 7 disposed on the surface of the chip interior to the input/output pads. Bumps 5 are disposed on the pads of the array.

2. A substrate 221 is formed with an array 204 of vias 210. The array 204 of vias 210 correspond in position to the array 4 of bumps 5 on the flip chip 1. The vias 210 each are filled with conductive material and conductive pads 207, 217 are provided on both ends of each via

210.

3. The flip chip 1 is bonded to the substrate 201 with the array 4 of bumps 5 on the chip being registered in alignment with the arrays 204 of vias 210 on the substrate 201.

4. The assembly is cleaned.

5. An encapsulant 220 is used to underfill the gap 221 between the flip chip and the substrate.

6. Chip scale package bumps 219 are applied to the bottom of the substrate 201.

From the foregoing, it can be seen that a significant advantage of the invention it that standardized arrays may be developed on substrates which will permit different flip chip circu designs to utilize standardized chip scale package substrates. This has the benefit and advant that low cost substrates may be utilized and that coarser bumps may be used .

The invention has been described in terms of an illustrative embodiment. As will be apparent to those skilled in the art, various changes and modifications may be made to the structure and to the method of the illustrative embodiment without departing from the spirit a scope of the invention. Accordingly, it is intended to limit the scope of the invention only by the following claims.

Claims:

1. A flip chip assembly (200), comprising:

an integrated circuit (1) comprising a die having a first length and a first width, an active circuit (2), said active circuit having a plurality of input/output pads (3) distributed adjacent the periphery of said die, an array of contact pads (7) disposed interior of said periphery, each of said contact pads being connected to a corresponding one of said input/output pads by a metallization path (8), and first bumps (5), each of said first bumps being disposed upon a corresponding one of said interior contact pads;

a substrate (201) having a second length and a second width, said substrate further comprising a plurality of vias (210), each of said vias comprising conductive material and being disposed on said substrate so as to be in alignment with a corresponding one of said first bumps, each of said vias being affixed to said corresponding one of said bumps at one surface of said substrate, said substrate carrying a plurality of second bumps (219) on a second surface opposite said first surface, each of said second bumps being disposed on a corresponding one of said vias.

2. A flip chip assembly in accordance with claim 1, comprising:
an underfill (220) disposed between said die and said substrate.

3. A flip chip assembly in accordance with claim 1, wherein:
said first bumps (5) each comprise a solder alloy.

4. A flip chip assembly in accordance with claim 3, wherein:
each of said first bumps (5) is gold plated.

5. A flip chip assembly in accordance with claim 1, wherein:
each of said first bumps (5) is gold plated.

6. A flip chip assembly in accordance with claim 1, wherein:
each said via (210) is filled with said conductive material.

7. A flip chip assembly in accordance with claim 1, comprising:
a solderable contact (207) formed on each said via at said substrate first surface.

8. A flip chip assembly in accordance with claim 1, comprising:
a solderable contact (217) formed on each said via at said substrate second surface.

9. A flip chip assembly in accordance with claim 8, comprising:
a solderable contact (207) formed on each said via at said substrate first surface.

10. A flip chip assembly in accordance with claim 1, wherein:

each said via (210) comprises a plated thru hole.

11. A flip chip assembly in accordance with claim 10, comprising:

a solderable contact (207) formed on each said via (210) at said substrate first surface.

12. A flip chip assembly in accordance with claim 10, comprising:

a solderable contact (217) formed on each said via (210) at said substrate second surfa

13. A flip chip assembly in accordance with claim 1, wherein:

said substrate second length is no greater than 120% of said die first length, and said substrate second width is no greater than 120% of said die first width.

14. A method of assembling an integrated circuit device (200) comprising an integrate circuit chip (1) having input/output pads (3) disposed adjacent to the periphery of said chip, comprising the steps of:

redistributing said input/output connections of said chip by forming an array of conduc pads (7) on one surface of said die, said array of pads being disposed interior to the periphery said die and a conductive pattern (8) on said one surface to establish connections between sai input/output pads and corresponding ones of said conductive pads,

forming a bump (5) on each of said conductive pads;

affixing said chip to a substrate (201), said substrate having formed therein an array of conductive vias (210) each extending from a first surface of said substrate to the opposite surface. of said substrate and each via disposed to be in registered alignment with a corresponding one of said bumps; and

forming second bumps (219) on said opposite substrate surface for attachment to a circ

15. A method in accordance with claim 14, comprising:

underfilling between said die and said substrate.

16. A method in accordance with claim 14, comprising:

underfilling between said die and said substrate with an epoxy material (220).

17. A method in accordance with claim 14, wherein:

said substrate (201) has a length not exceeding the length of said die by more than 20% and having a width not exceeding the width of said die by more than 20%.

18. A method in accordance with claim 14, comprising:

filling each said via (210) with conductive material.

19. A method in accordance with claim 14, wherein:

said substrate (201) is at least the size of said die (1) and no greater than 120% of the size of said die.

FIG. 1

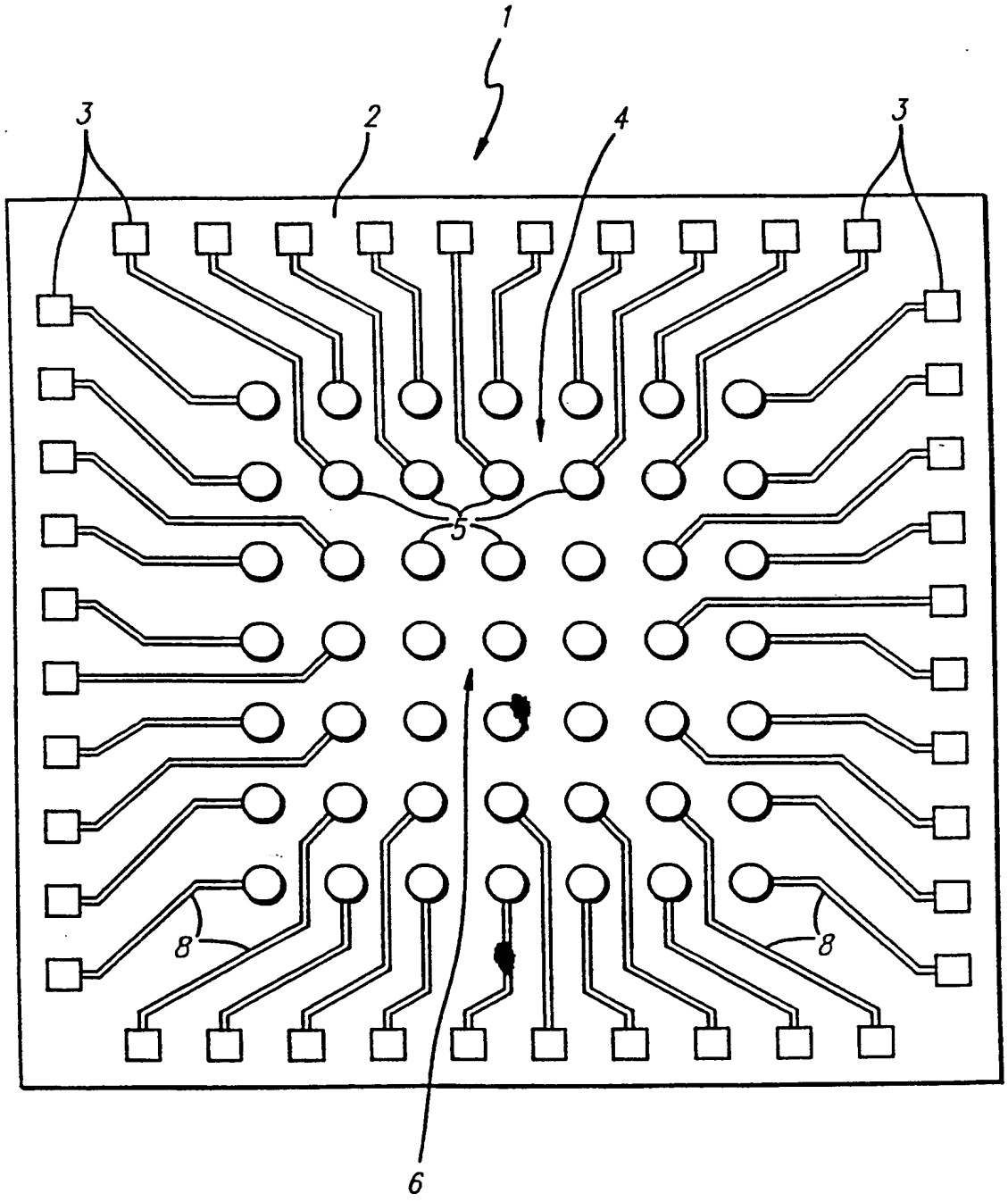

FIG. 2

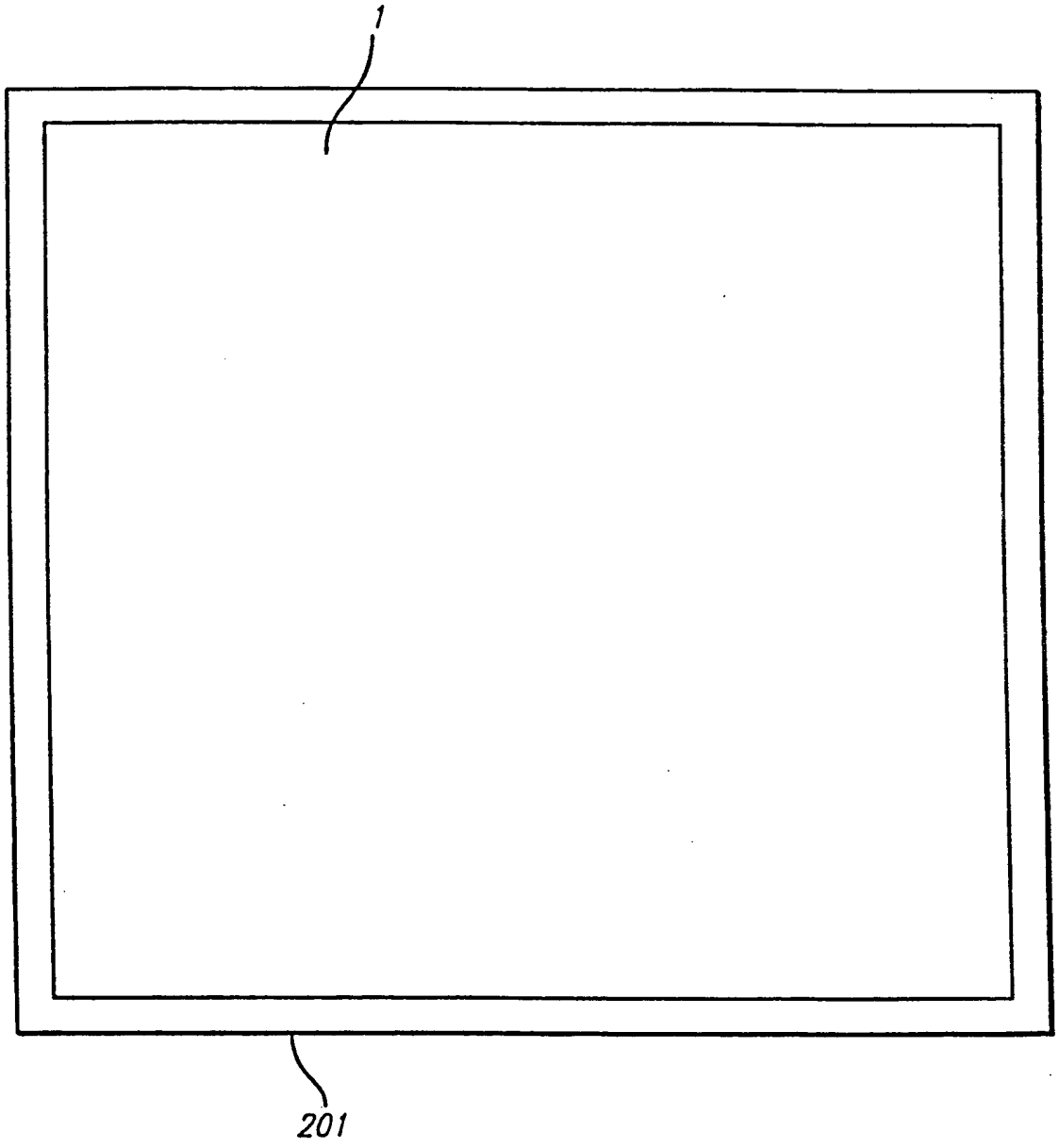

FIG. 3

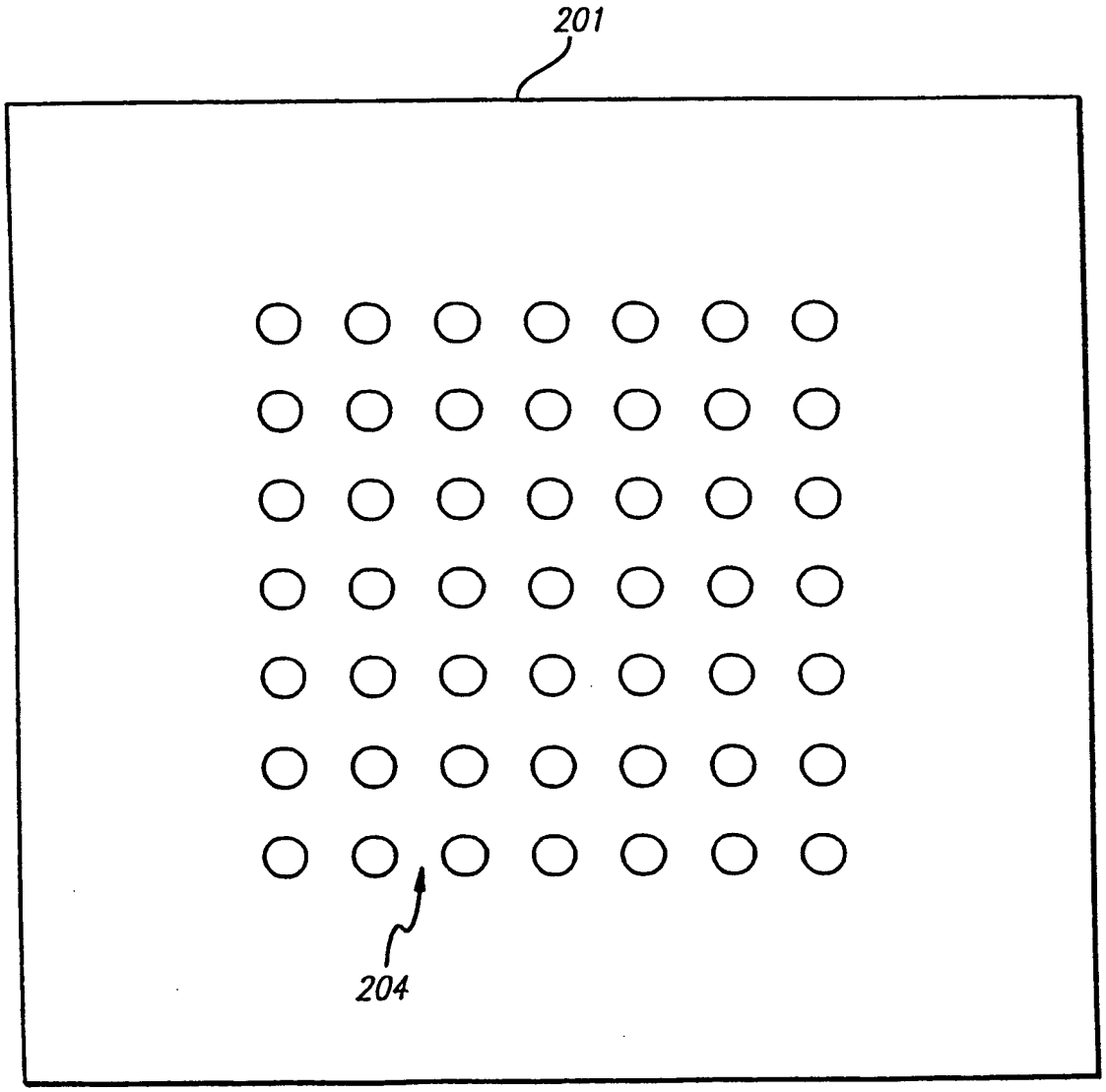

FIG. 4

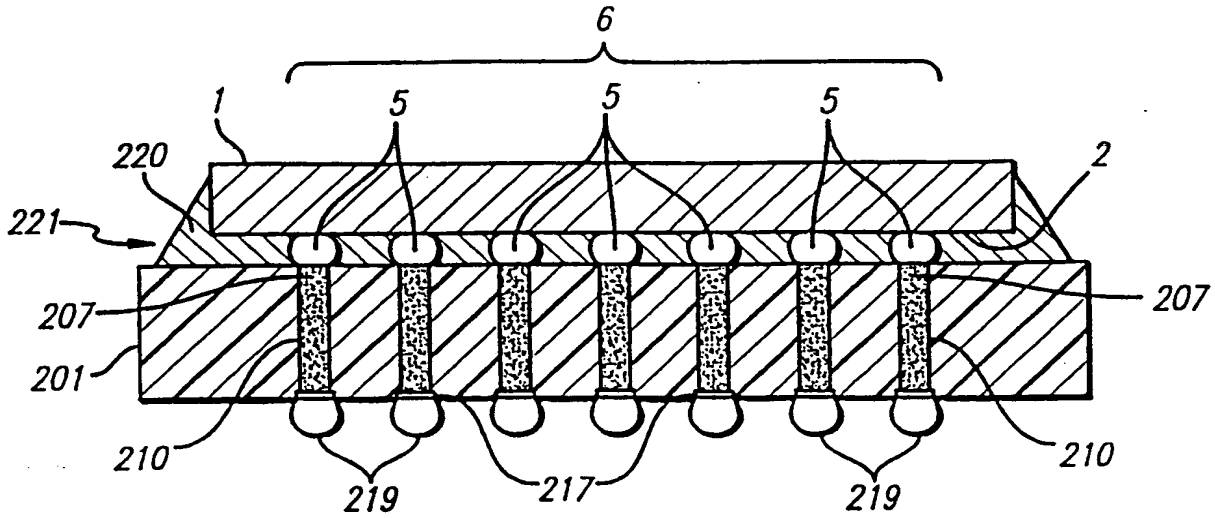
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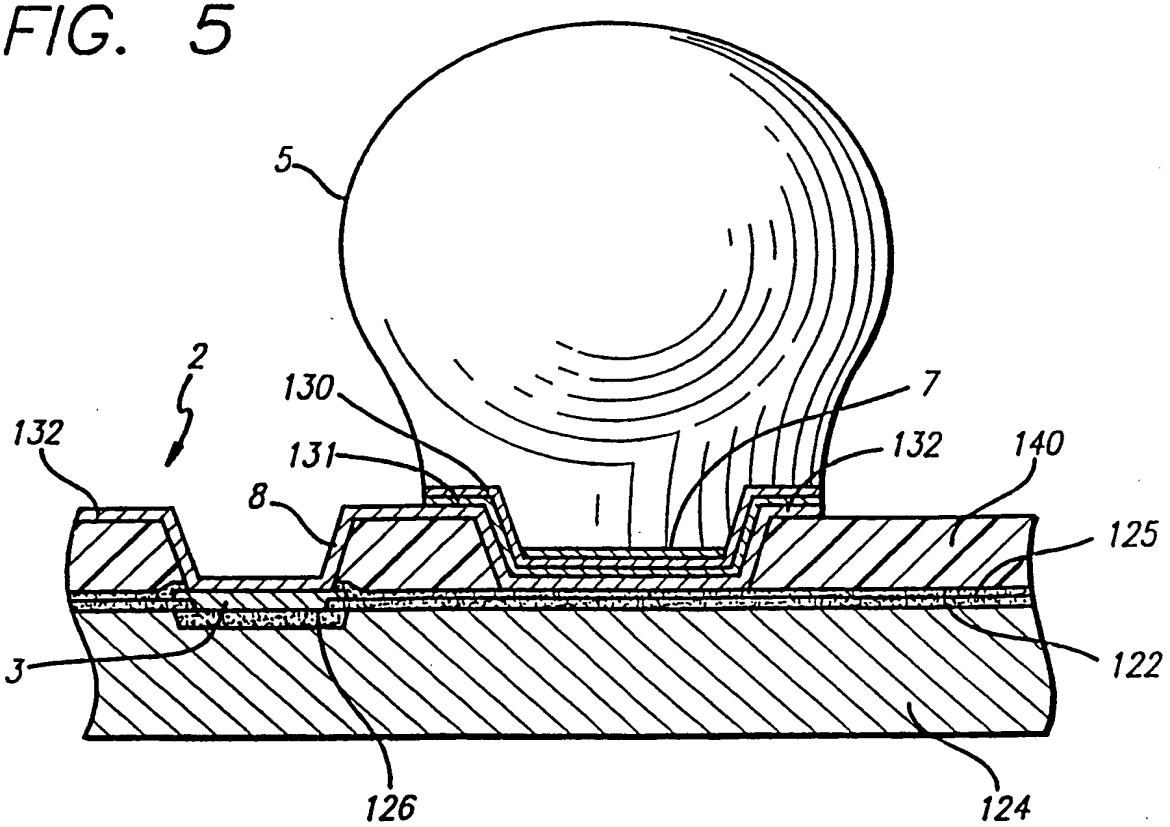
FIG. 5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